Research and Design of High-speed Camera Trigger Circuit for CO2 Protection Welding Monitoring System based on FPGA

Zhiyong Jiang

Practice teaching department, Guilin University of Aerospace Technology, Guilin, China

972881263@qq.com

Abstract. In the monitoring system of CO2 protection welding, based on the change of current waveform during short-circuit transition of CO2 protection welding, a trigger circuit of high-speed camera shutter is developed and designed, which can trigger the high-speed camera to take welding pool image at the right time, so as to obtain clear and non-interference photos and videos of welding pool, which has been verified in the experiment.

Keywords: CO2 protection welding, short circuit transition process, high-speed camera, trigger, FPGA.

1. Introduction

Among all metal processing methods, welding processing quantity is in the forefront. There are four common types of droplet transfer for all molten-pole arc welding, among which short-circuit transfer is one of them [1]. Short circuit transition is suitable for all position welding and thin plate welding. This kind of transition mode is usually carried out under the conditions of small current, low voltage and fine wire, and CO2 is usually used as protective gas. Short-circuit transition process and welding current and arc voltage waveforms are shown in Fig.1 [2]. When short-circuit transition occurs, the arc length is relatively short, and the melting droplets at the end of the welding wire contact with the surface of the molten pool before they become large droplets. When the arc is extinguished, the droplets are rapidly separated from the end of the wire and transferred to the molten pool under the combined action of electromagnetic contraction force and surface tension of the molten pool. Then the arc ignites again, repeating the above process. Common welding monitoring system consists of high-speed camera, acquisition card, computer system and image processing software. The acquisition of clear and non-interference molten pool image and video is the basis of effective work of welding monitoring system. Because of the strong arc, spatter and smoke during the short-circuit transition process, the pool photos and videos obtained in the CO2 protection welding monitoring system are disturbed, and the noise and strong light are serious.

In Fig. 1, T is the time of a short-circuit transition period, Tr is the time of arc combustion, and Td is the time of short-circuit transition. Corresponding to time 1-8, the state of short-circuit transition process is as follows: time 1, forming neck, about to break; time 2, reburning arc; time 3, arc burning; time 4, arc length gradually shortened; time 5, about to short-circuit; time 6, starting short-circuit, forming bridge; time 7, forming neck, about to break; time 8, reburning arc. In the monitoring system, the high-speed camera is responsible for the acquisition of images and videos. If the camera shutter is opened at Tr during the arc combustion period, the image of molten pool is blurred due to the influence of arc light, smoke and spatter, as shown in Fig. 2.

According to the waveform of welding current, if the pool image is taken by Td in the short-circuit period without arc and spatter, then the obtained photos can be clear and free of interference. So, a special trigger can be designed to control the shutter opening of high-speed cameras, and the trigger pulse of the shutter opening of cameras can be generated by Td in short-circuit period.

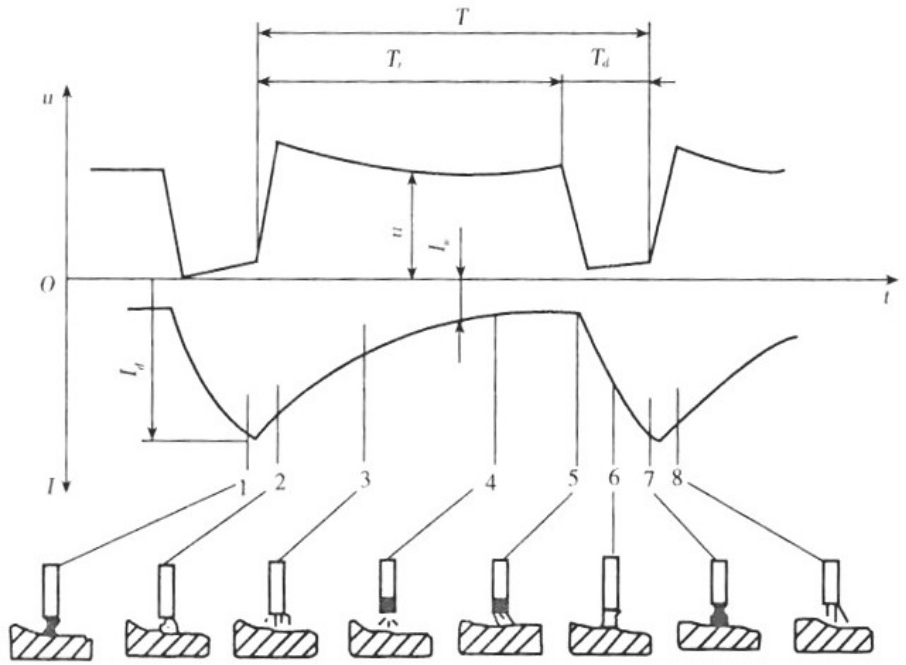

Fig 1. Short Circuit Transition Process and Welding Current and Arc Voltage Waveform

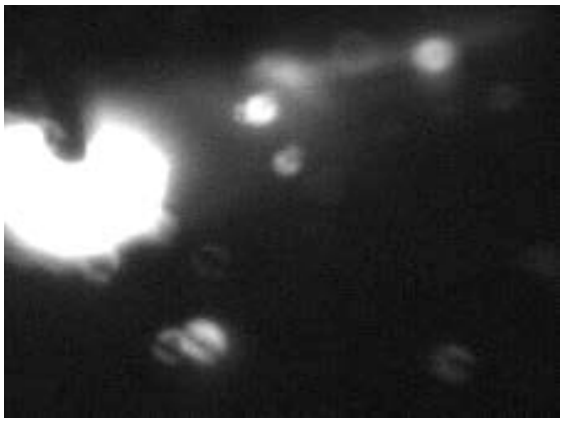

Fig 2. Molten pool image (camera shutter self-triggering)

2. Scheme Composition and Circuit Design

The system hardware block diagram is shown in Fig. 3.

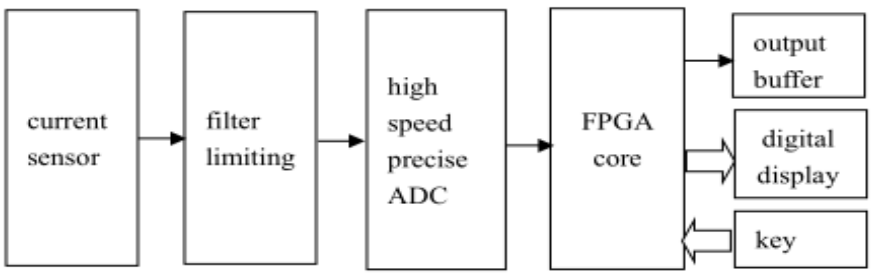

Fig 3. system hardware block diagram

2.1 Signal Input and Impedance Matching Circuit

The input signal of the system is from the current sensor. When the welding machine is short-circuit welding normally, the working current is generally about 80-200A, and the short-circuit transition frequency of droplets is generally 20-200 times/s [3]. So, the type of current sensor used is LHK-200A, which has integrated current-to-voltage conversion circuit. It requires

±12V DC power supply, maximum conversion current 200A, output ±5V signal, output voltage and measurement circuit have changed linearly. The impedance matching circuit is very necessary because of the connection attenuation in the signal circuit and various disturbances in the experimental and industrial production environment because of the use of 4-meter or so 4-core shielded wire to transmit signals and provide DC power for the sensor. The design circuit uses first-order LM358 to improve the input impedance. The circuit is shown in Fig. 4.

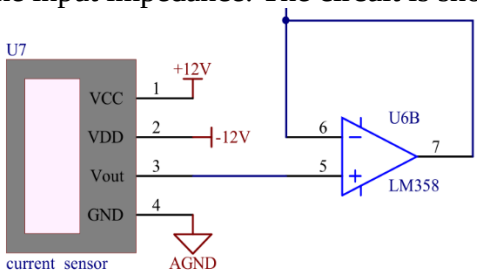

Fig 4. Current Sensor and Impedance Matching Circuit

2.2 Filter and Limiting Circuitt

As shown in Fig. 5, R12 and C34 constitute a first-order low-pass filter with a cut-off frequency of 10 KH_Z, which guarantees a low phase difference of 3 degrees at 250 HZ, equivalent to a delay of 33 μs. It can also filter out high frequency interference. Two Zener diodes, D2 and D4, are used to limit the amplitude and protect the input port of AD. The output buffer of U6A voltage follower reduces the influence of the front circuit on AD.

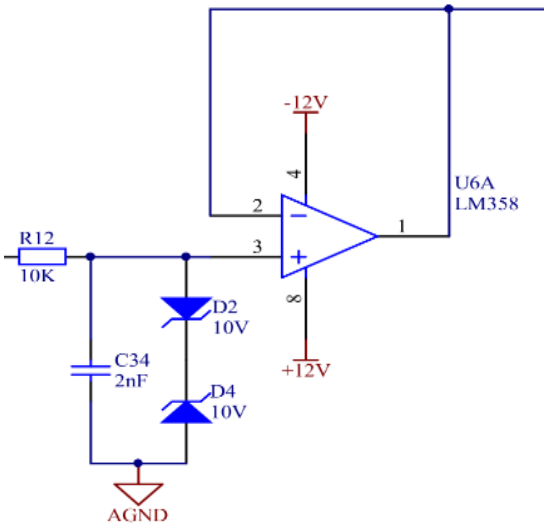

Fig 5. Filter and limiting circuit

2.3 ADC Circuit

ADC uses ADS8515, which is a 16-bit high-speed parallel ADC with the highest sampling rate of 250 KSPS [4].5V provides power for analog part of the chip. The signal can be input between + 10V and - 10V. The precision is 0.3mV. The precision requirement can be achieved without AGC circuit. 3.3V power supply for chip digital system can avoid the level matching problem between ADC chip and FPGA. The circuit is shown in Fig. 6.

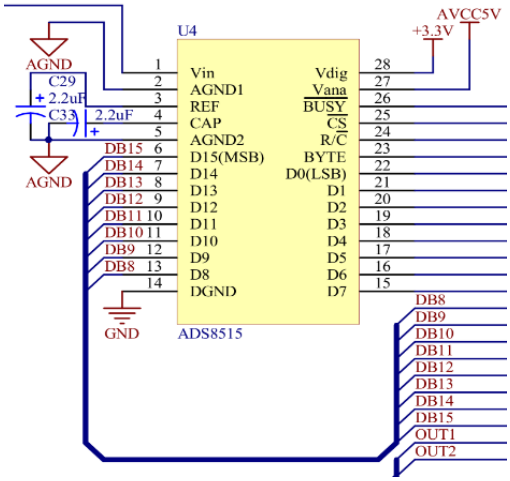

Fig 6. ADC circuit

2.4 FPGA Core and Related Circuits

The core of system control is EP2C5T144I8N with 4608 LE [5]. Its internal resources are enough to meet the design requirements.

The configuration chip of the FPGA is EPCSISI8. The power-on loader can be implemented in the FPGA [6], and the power-off and maintenance of the FPGA program can be realized.

2.5 Output Buffer Circuit

3.3V and 5V bus buffers are SN74LVC4245A, which can realize output buffering and TTL level matching. The circuit is shown in Fig. 7.

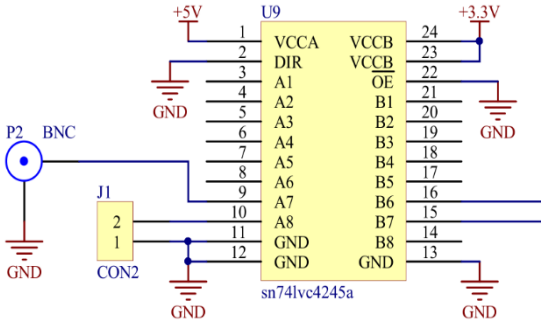

Fig 7. Output Buffer Circuit

2.6 Digital Tube and its Driving Circuit

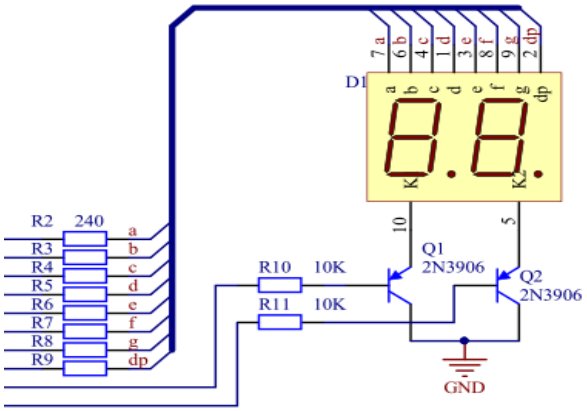

Fig 8. Digital Tube and Its Driving Circuit

The digital tube adopts two-position common cathode digital tube, which displays keys and preset values by dynamic scanning mode, and the cathode driver adopts triode 2N3906. The circuit is shown in Fig. 8.

3. FPGA Software Composition Block Diagram

The software block diagram is shown in Fig. 9.

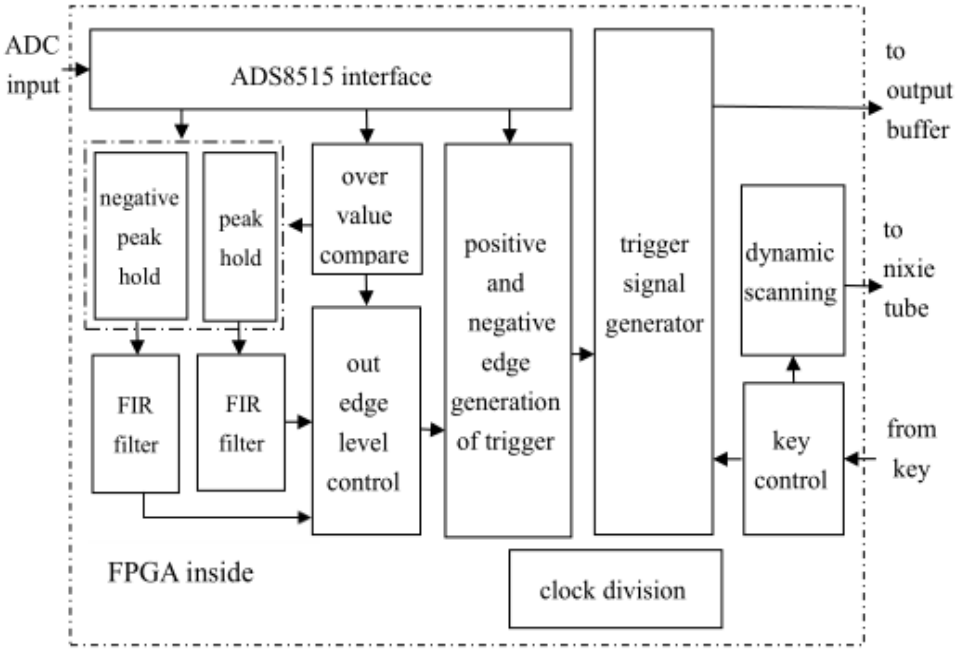

Fig 9. FPGA software composition block diagram

3.1 ADS8515 Interface Module

ADS8515 interface module. The circuit controls ADS8515 chip to convert sensor signal to 16-digit AD data [15.0] at 100K conversion rate. The interface clock is generated by clock frequency division module, and data exchange with ADS8515 is shown in the fig.10. Data obtained from ADS8515 are transmitted to negative peak holding, peak holding, over-value comparison, positive and negative edge generation circuit module of flip-flop.

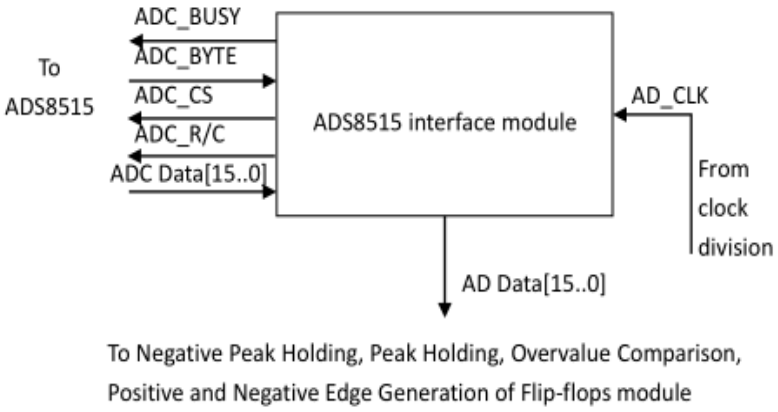

Fig 10. ADS8515 interface module

3.2 Negative Peak Holding Module

The negative peak holding circuit has 16 bits of data input and 16 bits of data output. The lowest voltage in each cycle is obtained through the internal comparator of the module, and the FIR of the

digital low pass filter is used. S-CLK is the peak value of module asynchronous zero-clearing, and the asynchronous update signal is generated by zero-crossing comparator, which is used to update the peak data in each signal cycle. Output Min [15..0] is not affected by S_CLR. Min [15..0] latches updates when the peak signal is generated.

3.3 Peak Holding Module

The peak holding circuit has 16 bits of data input and 16 bits of data output. The maximum voltage in each cycle is obtained by the internal comparator of the module, and the FIR of the digital low pass filter is used. S-CLK is the peak value of module asynchronous zero-clearing, and the asynchronous update signal is generated by zero-crossing comparator, which is used to update the peak data in each signal cycle. The output MAX [15..0] is not affected by S-CLR. MAX [15..0] latches the update when the peak signal is generated.

3.4 FIR Filter Module

FIR filter module is a two-channel finite impulse response low-pass digital filter with a cut-off frequency of 10 Hz [7], which is used to reduce the interference of welding process photography to the system.

3.5 Overvalue Comparison Module

Over-value comparison module through the internal Schmidt comparator, when AD-Data is greater than a fixed value, the rising edge, when less than a fixed value, the falling edge, so that the post-circuit can correctly detect the phase.

3.6 Outbound Level Control Module

The output edge level control module can output the data value of the trigger outlet edge in proportion to the peak value.

3.7 Positive and Negative Edge Generation Module of Flip-flop

The positive and negative edge generation module of flip-flop is a double-limit comparator. When the data AD-Data [15..0] sampled by AD is larger than that of D-up [15..0], the output edge of the module rises; when the data AD-Data [15..0] is smaller than that of D-down [15..0], the output edge of the module falls.

3.8 Trigger Signal Generation Module

The trigger signal generating module counts the pulses generated by the trigger compiling and generating module, and outputs the final output signal.

3.9 Key Control Module

The trigger signal generation module controls the output of C-Data from 0 to 99 by processing the key value.

3.10 Dynamic Scanning Module

Dynamic scanning module drives two digital tubes to display the value of C-Data [5.0] by dynamic scanning mode.

3.11 Clock Frequency Division Module

The 50MHZ crystal oscillator clock frequency is divided into the clock frequency needed by each module.

4. Measured Waveform

After the design and manufacture of the trigger is completed, it is connected to the welding monitoring system. The shutter of the high-speed camera is triggered by the trigger (the rising edge is adjustable in the camera). The current waveform of the current sensor and the corresponding trigger output waveform are measured as shown in the figure. CH1 is the welding current waveform output by the current sensor, CH2 is the trigger waveform generated by the trigger corresponding to the trigger, and the trigger pulse of the rising edge is generated along the descending edge of the welding current, and the level is TTL. The measured current waveform and the output waveform of the trigger are shown in Fig. 11.

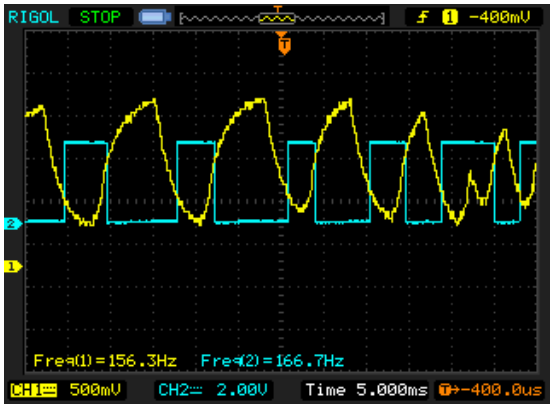

Fig 11. Measured Current Waveform and Trigger Waveform

5. Practical Application Effect

After the design and manufacture of trigger is completed, it is applied in the welding monitoring system. Comparing the image of molten pool obtained by the trigger shutter of the camera itself (as shown in Fig. 2) and the image of molten pool obtained by the trigger shutter made by this design (as shown in Fig. 12), it can be seen very clearly that the image of molten pool shown in Fig. 2 is just in the Tr time period shown in Fig.1, approximately around time 3, when the arc burns, there is arc light and spatter, so the shape of molten pool is not blurred. Clear. The image of the molten pool shown in Fig. 12 shows no arc and splash, and the shape of the molten pool is very clear. The welding quality can be clearly judged according to the shape of the molten pool, which provides a good condition for the further development and application of the welding monitoring system.

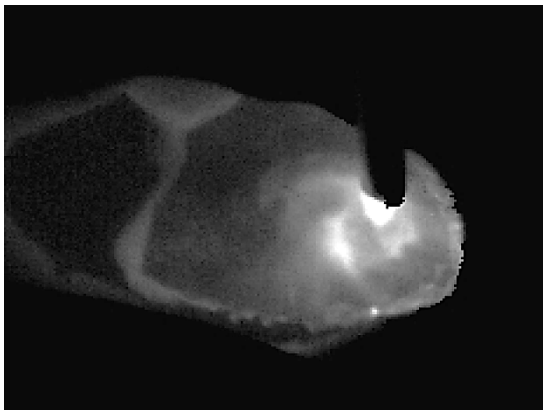

Fig 12. Molten pool image (trigger trigger camera)

6. Conclusion

In the monitoring system of CO2 protection welding, based on the change of current waveform during short-circuit transition of CO2 protection welding, a trigger circuit of high-speed camera shutter is designed and manufactured with the core of FPGA, which solves the problem of trigger opening time of high-speed camera shutter, and is applied in the actual monitoring system. It

provides a good way for the monitoring system of CO2 protection welding to obtain clear and stable molten pool image.

Acknowledgments

This work was financially supported by Director Fund of Key Laboratory of Robot and Welding Technology in Guangxi Universities (JQR2017ZR01) and Basic Competence Promotion Project for Young and Middle-aged Teachers in Guangxi Universities(2017KY0862).

References

[1] Howard B. Cary, Scott C. Helzer, translated by Chen Maoai, Wang Xinhong, Chen Junhua, Qi Yongtian, Lu Xiaoling, Li Qingming, et al. Modern Welding Technology, 6th ed., Beijing: Chemical Industry Press, 2010, p86.

[2] Qiu Jiafei, Cai Cenying, Practical Welding Technology--Welding Process, Quality Control, Skills and Textual Research Competition, Changsha: Hunan Science and Technology Press, 2010, p104.

[3] Chinese Mechanical Engineering Society Welding Society, Welding Manual Vol. 1, Beijing: Machinery Industry Press, 2007, p162.

[4] Texas Instruments, ADS8515 DataSheet, http://www.ti.com/lit/ds/symlink/ads8515.pdf.

[5] Yu Le, Xie Yuanlu, Design and Implementation of FPGA Chip Architecture, Beijing: Electronic Industry Press, 2017, p278.

[6] Intel, EP2C5T144I8N datasheet, https://pdf1.alldatasheet.com/datasheet-pdf/ view /527246 / ALTERA/EP2C5T144I8N.html.

[7] Arthur B. Willians, Fred J. Taylor, 4th ed., translated by Ning Yanqing, Yao Jinke, Electronic filter design handbook, Beijing: Science Press, 2008, p380.